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Delta-Sigma Modulators
Noise Sources in Switched-Capacitor
Mismatch-Induced Noise

Quantization Noise (Quick Review)

Clock Jitter Induced Noise (DT and CT Systems)

Flicker Noise (CDS, Chopper Techniques)

Thermal Noise

General Overview of Noise Sources in Delta-Sigma Modulators

Noise Source in SC Delta-Sigma Modulators

Outline for This Presentation
Noise Sources in a SC Delta-Sigma Modulator
The performance is virtually insensitive to errors that occur in the proposed feed-forward signal path (except when the OSR is extremely low). Errors that occur in subsequent stages of the loop filter are of less concern, as they are suppressed by the gain from $e$ to the respective node. Generalizing and subtracting $\tilde{g}(y)$ from $a(y)$ is a very critical process.

Any errors, including noise, in $e(y)$ will adversely affect the performance. The modulator’s sensitivity to errors spans from “severe” to “negligible.”

To enable meaningful comparisons, all errors will be referred to the input.

Nodes that are sensitive to imperfections.
When idle tones are expected, we want: \[ P(T_N) > P(W_N) + P(I_N) + P(D_N) + P(Q) \]

Low power consumption: \[ P(T_N) = P(W_N) + P(I_N) + P(D_N) + P(Q) \]

The power consumption is generally determined by \[ P(T_N) \]

For SC implementations, \[ P(T_N) \] is inversely proportional to \( OSR \cdot C \)

\[ \frac{P(W_N) + P(I_N) + P(D_N) + P(T_N) + P(Q)}{S} = P\left( \frac{N}{S} \right) \]

\( f \rightarrow f_S f = N \)
is critical for modulators based on a continuous-time feedback signal
\[ f_N \]
depends on the derivative of the signal with respect to time
\[ f_N \]
is strongly signal-dependent for high signal levels (stability issue)
\[ \partial N \]
can often be reduced by using Chopper and/or CDS techniques
\[ p_N \]
Reducing by 3 dB generally implies doubling the power consumption
\[ q_N \]
and are generally \( p_N \) and \( q_N \) (but not always) independent of the signal level
\[ S \]

Noise Components may Depend on the Input Signal

\[ SNR \]
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Outline — Progress
This is a key result, which will be used repeatedly in this lecture.

\[
\frac{\mathbb{E}_X}{\mathbb{D}_P} = \int_0^\infty f P_{T}^{(\theta)}(\theta) \frac{1}{\mathbb{D}_P} = \int_0^\infty f P_{T}^{(\theta)}(\theta)^{\mathbb{M}} \mathbb{D}_P = \frac{\text{Power}}{\text{PSD}} \int_0^\infty \mathbb{I}^{(\theta)}(\theta)^{\mathbb{M}} \mathbb{D}_P
\]

The power of \( (\theta)^{\mathbb{M}} \) is finite, which we can calculate as follows:

\[
\frac{\mathbb{E}_X}{\mathbb{D}_P} = \frac{\mathbb{E}_X}{\mathbb{D}_P} = \mathbb{E}_X \cdot \mathbb{D}_P = (f)^{\mathbb{M}} \mathbb{D}_P
\]

The time constant \( T \) and the gain in the pass band is a filtered version of \( X \) using a single-pole low-pass filter with power spectral density \( P_{\mathbb{D}} \), and hence has infinite power.

\( (\theta)^{\mathbb{M}} \) is a theoretical white noise signal with infinite bandwidth, constant noise power.

When sampling a single-pole noise signal
\[ \left\{ \frac{\gamma}{X} \right\} \bigwedge \text{PSD} \quad \mathcal{N} \in (\gamma)^u \Lambda \quad \text{and} \quad \frac{S_f}{\text{PSD}} \cdot \frac{\gamma}{X} \bigwedge \text{PSD} = \frac{S_f}{\text{PSD}} \bigwedge \text{PSD} = (\gamma)^u \Lambda \]
Assuming that \( R \cdot \mathcal{C} \lesssim S_{\text{PSD}} \), we know that \( \left( \gamma + 1 \right) \mathcal{A} \) and \( \gamma \mathcal{A} \) are uncorrelated, hence:

\[
\frac{\mathcal{C}}{\mathcal{Y}} = \frac{\mathcal{RHF}}{\mathcal{HFHF}} = \frac{1}{(0 = f) \mathcal{A}} = \frac{1}{\text{PSD}^{\gamma}} \]

Utilizing the results we have derived, we can now find very easily

\[
\mathcal{R} = \text{The PSD of } \mathcal{A} \text{ at low frequencies is } \mathcal{HFHF} \]

\[
\mathcal{A} \cdot \mathcal{C} = \text{The filter's time constant is } \text{HFW}^{\gamma} \]

\[
\mathcal{R}^{\gamma} = \text{The thermal noise component for the resistor is described by } \text{PSD}^{\gamma} \]

Example: Deriving the Famous "KT/C" Result
The objective is to determine the noise when used in a SC DSM application in a continuous-time configuration, e.g., a unity-gain configuration.

You can use SPICE to determine the input-referred noise level of your opamp.

(\frac{P_I}{qw} \propto \frac{w_\beta}{\varepsilon/\varepsilon})

Low noise generally implies high power consumption (because of high noise).

In that case, the input-referred noise is PSD will be approximately

When designed for low-noise, the differential pair transistors should dominate

All transistors contribute to the input-referred thermal noise.

Thermal Noise in Operational Amplifiers
\[
\frac{C/(y) e^{-e}}{\text{rms}} \left[ (y)^{p} A \right] = \text{SNR}
\]

Refer it back to the input signal as follows.

Once we have calculated the thermal noise component \( e \), we may

\[
(y)^{p} A \cdot \int \mathcal{C} = (y)^{s} \cdot (y)^{e} \cdot \int \mathcal{C} = (y)\mathcal{C}^\text{out}
\]

\[
\int_{0}^{\infty} \frac{dQ}{Q} = (y)^{e} \cdot \int \mathcal{C} \cdot \mathcal{C}^\text{out}
\]

The derived signal component \( (y)^{s} \) is the charge pulse signal being integrated. The calculations are derived most effectively by first focusing on \( e \).

\[
(y)^{e} \cdot \int \mathcal{C} = (y)^{s} \cdot \int \mathcal{C} + (y)^{e} \cdot \int \mathcal{C}^\text{out}
\]

Clock Phase \( \Phi \)

Clock Phase \( \Phi \)

Thermal Noise in the Input Stage of a SC DSM
\[
\frac{C}{L} = \frac{(Z_{SW} + R + i R)(C L)^{1/2}}{\sqrt{Z_{SW} + R}} = \frac{\text{PSD}(0)}{\text{PSD}} = \frac{\text{ms}[\Delta f \lambda_{\text{rms}}^2]}{2^{1/2}} 
\]

Alternatively, we may express the result in the voltage domain by the input signal \( \lambda \):

Noise stored as voltage/charge on capacitor \( C \) will cause a charge transfer, counted as offset contributions, and not as noise contributions. Deterministic effects, such as non-stochastic charge injection, should be included.

\[
\lambda_\text{rms} \approx \left( \frac{\lambda \cdot \Delta f}{C} \right)^{1/2} 
\]

Thermal noise due to resistance in the switches will unavoidably cause stochastic variations in \( \lambda \) which will typically cause surprisingly high noise in the voltage/charge stored on the capacitor \( C \)

Nominally, the voltage signal \( \lambda \) is

\[
\frac{\Delta f}{C} \lambda_{\text{rms}} \lambda_\text{rms} 
\]

Clock Phase 1 - Clock Phase 2
\[ S_f \cdot b \cdot \ln(2) \cdot N \leq \frac{T_{bw}}{I} \]

The system must settle to \( N \) bits of precision within \( T_{bw} \) of clock phases.

For any design, however, you have an a priori knowledge of the value of \( T_{bw} \)

\[ \left( \left( \frac{T}{T} \right) \left( \frac{P}{P} \right) \right) \]

can be determined quite easily using SPICE (plot the current \( I/T \)).

Do not blindly assume that all noise contributions are of the form \( 1/T \).

There is not a fundamental relationship between \( T_{bw} \) and the noise PSD.

The bandwidth of the opamp and the feedback factor do not affect the

continuous-time dynamics of \( e(t) \).

It is necessary to first consider the

so we will cover it piecemeal.

There is a lot going on in phase \( \phi \).
Do not use a opamp that is faster than necessary. 

\[
\left\{ \frac{m_{\text{BW}}}{P_{\text{SDAMP}}} \right\} \mathcal{N} \equiv (\gamma)^{\text{AMP}} \frac{V_{\text{BW}}}{C_{\text{Z}}}.
\]

Conclude that \( \text{AMP} \) is a white noise signal \( \mathcal{N} \) and the next, and hence we conclude that the system settles fully \( \text{BW} \) is the total power of the low-pass filtered white noise signal having a total power of

\[
\frac{w_{\text{BW}}}{S_{\text{BW}}} \frac{1}{C_{\text{Z}}} \approx \frac{w_{\text{BW}}}{P_{\text{SD}}} \frac{1}{C_{\text{Z}}} = \frac{w_{\text{BW}}}{P_{\text{SD}}} = \text{rms}^2 \left[ (\gamma)^{\text{AMP}} \right] \text{BW}.
\]

Given that the system settles fully, we deduce that there is virtually

\[
\frac{w_{\text{BW}}}{S_{\text{BW}}} \frac{1}{C_{\text{Z}}} \approx \frac{w_{\text{BW}}}{P_{\text{SD}}} \frac{1}{C_{\text{Z}}} = \text{rms}^2 \left[ (\gamma)^{\text{AMP}} \right] \text{BW}.
\]

Based on the (very reasonable) assumption that you have designed the system to have a first-order settling behavior (characterized by \( \text{BW} \)), we find that

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\]

The thermal noise analysis to find/estimate

\[\text{Thermal Noise Analysis - Opamp}\]
where \( f_p^{(j)*\Theta} \) are the "aliasing" frequencies

\[
\int_{-f}^{f} P(f) e^{-2\pi f T_o} df = \frac{1}{2} \int_{-\infty}^{\infty} \left[ p(y) * \Theta \right] e^{-2\pi f T_o} df
\]

use SPICE to estimate the PSD of the induced noise signal \( \Theta \). If the time constant of the noise component induced in \( \Theta \) by the reference voltage buffer does not meet the previously derived result, \( T_o \) is not determined by output capacitance (then the bandwidth of \( \Theta \) is not determined by opamp).

Some designs use a slow reference-voltage buffer driving a large external load \( \frac{V_{\text{r}}}{P_{\text{r}}^{(j)*\Theta}} \). The fast voltage reference buffer facilitates full integration, but care must be taken to assure proper single-pole settling. A fast voltage reference buffer can be designed in several different ways, and the noise characteristics may be very different.

The reference voltage buffer can be used to implement the DAC.
The switches' impedance and PSD is thus increased gradually, and the system's bandwidth will eventually be limited by the switches' impedance.

By choosing $R_{SW3} + R_{SW4}$ sufficiently small, we can achieve $\frac{P_{SD}}{Q_{1}} \approx \frac{\sum_{n=1}^{\infty} f_{n}(\omega) e^{-jx}}{\sum_{n=1}^{\infty} f_{n}(\omega) e^{-jx}}$.

We may thus (correctly) estimate that the bandwidth can be estimated in the manner described earlier:

$\frac{\sigma_{P_{SD}}}{\sigma_{Q_{1}}} \approx \frac{P_{SD}}{Q_{1}} \cdot \frac{\sum_{n=1}^{\infty} f_{n}(\omega) e^{-jx}}{\sum_{n=1}^{\infty} f_{n}(\omega) e^{-jx}}$.

The induced noise's PSD at low frequencies is potentially very decaying.
Note that $g_m \cdot T_{bw}$ is a capacitance. Typically,$$
abla \frac{\text{OSR}\cdot C}{N_f T} > \frac{1}{\sqrt{L^2}} \quad \text{Typically} \quad \frac{\text{OSR}\cdot C}{N_f T} \sqrt{[\Delta f^d A]} \approx \frac{\text{PSD}_{\text{amp+psd}}}{\text{rms}} \sqrt{[\Delta f^d A]} \frac{C_{\text{osr}}}{\text{rms}} \frac{\text{PSD}_{\text{amp}}}{\text{rms}} [\Delta f^d A] = \text{SNR} \quad \text{dB}
$$

The signal-to-noise ratio (SNR) can thus be calculated as

Only a fraction $\frac{1}{\text{OSR}}$ of the power in the signal band is located in the signal band.

The cumulative white noise component comprised in $\Delta f$ is$$((y)^d A - (y)^* A) \cdot \text{C} = (y)^{sA} \quad \text{is comprised in } \Delta f$$

The signal component comprised in $\Delta f$ is $\sqrt{[\Delta f^d A]}$.

Summary

Thermal Noise Analysis

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Joseph Steenson
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\((1 + j\omega)dN \approx (j\omega)dN\) is low-frequency noise. \(dN\)

We can obtain this behavior by replacing \(0\) by \(j\omega\), or vice versa.

Ideally, the voltage variation on the capacitor's right-hand side would be zero.

Reducing may be expensive in terms of power and/or chip area.

Flicker noise enters the system in the same way as \(v_{\text{flicker}}\).

\[
\begin{align*}
& (\{0 - (j\omega)dN\} + [(j\omega)pA - (j\omega)eA]) \cdot I_C = \\
& (\{(j\omega)dN - (j\omega)pA\} - [0 - (j\omega)eA]) \cdot I_C = (j\omega)pA \cdot I_C = (j\omega)e
\end{align*}
\]

We may calculate the charge being integrated as...

\begin{itemize}
  \item Problem in CMOS
\end{itemize}
Certain CDS schemes have substantial advantages for highly nonlinear opamps. CDSS topologies do not support double-sampling operation. The opamp's thermal noise is sampled twice (same for all CDS schemes). The power consumption is increased.

Because it is low-frequency noise, we have $P_{\text{TH}} = (\gamma) \phi$. Essentially, $\gamma$ stores the offset and flicker noise component.

This basic CDS scheme was originally proposed by K. Nagara.

Correlated Double-Sampling (CDS) Techniques
Although first published in 1981, it has not been used "widely" until recently. A high sampling frequency can be achieved (double sampling is also feasible).

There is no thermal noise penalty.

A high sampling frequency is modulated to \( f_N / 2 \). It is filtered out in the decimation process.

Simplify "rotate" the differential amplifier in every clock period: \( y \Phi \) for \( k \) even.

This is surprising because such techniques are ideal for SC circuits.

Choppering techniques are best known for their use in continuous-time circuits.

Chopper Suppression of Flicker Noise
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OSRs of less than 10 are generally not very practical (any SC/SL circuit)

The anti-aliasing filter must be linear and low-noise as the modulator

The anti-aliasing filter's complexity is inversely related to the OSR

To avoid aliasing errors, we need to filter a CT signal prior to sampling it

Hence, only the sampling process is sensitive to clock jitter

The signal is a sequence of values with no inherent correlation with time

Sequence machines can be either analog, digital, or both

Discrete-time (DT) signal processing is implemented by sequence machines

Clock Jitter Induced Noise in DT Modulators
(\gamma)_{L^\nabla} \cdot [(s_L \cdot \gamma)v] \frac{ip}{p} = (\gamma)f_N

When Sampling a Signal - Broadband Jitter
It is quite a different story for band-pass modulators

\[ \frac{\text{SNR}}{\text{dB}} = \frac{\nu}{\text{OSR}^\gamma} \cdot \frac{\text{SNR}}{\text{dB}} = \frac{\nu}{\text{OSR}^\gamma} \cdot \frac{\nu}{\text{SNR}} \]

Calculating the in-band signal-to-noise ratio, we find (independent of \(A_0\))

where \(s_L = \text{OSR}^\gamma \), \(s_f = \frac{\nu}{\text{SNR}} \), and \(s_f = \frac{\nu}{\text{SNR}} \).

When \(s_f \gg 1\), we will thus consider a tone at the edge of the base band.

The system is most sensitive to clock jitter when \(|\eta| \gg 1\) is large.

\[ \sum_{N=0}^{\infty} (\nu)^n = \frac{1}{1 - \nu} \]

Estimating the power of \(N\) for

\[ (\nu)^n \]
\[ \text{rms} \left[ \frac{s_L}{\gamma \cdot L \cdot \Delta V} \right] \cdot \text{rms} \left[ (\gamma)p \cdot \Delta V \cdot H \right] = \text{rms} \left[ \frac{H}{\gamma^2} \right] \text{N} \cdot \int_{\mathbb{R}}^{L} \left[ \frac{H}{L} \right] \text{d}t \cdot \text{N} \left( 0, \Delta V \right) \]

Errors caused by the feedback DAC will not be suppressed.

Errors induced in the S/H process will be suppressed by the NTF (\( \gamma \)).

Errors induced by clock jitter will occur only in the DT/CT/DT interfaces.

Clock Jitter Induced Noise in CT Modulators
a very good crystal clock and/or a high-resolution signal representation

For an aggressively designed modular I 1 and a

For a conservatively designed modular $H \frac{1}{1} = \infty$

and we have

and we find

let

will be an integer number of $g_{\text{lsb}}$ where for an $N$-level quantizer

**Clock Jitter Induced Noise in CT Modulators**
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Outline - Progress
amplitude – affects dynamic range. 

Tradeoff between suppression of 

high gain in the signal band. We need is a loop filter with very low 

system must be made stable, all bounded. Assuming PSD (\(u(x)\)) is bounded. 

Assume PSD (\(y(x)\) is bounded.

How to Suppress \(N_0\) in the Signal Band.
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The power of $G(x)$ is signal-dependent, it is maximum for small input signals.

$$\mathbb{E}[y] \cdot \mathbb{E}[y]^{\circ} = \int_{-\infty}^{\infty} \mathbb{E}[y] \cdot \mathbb{E}[y]^{\circ} \, dy = \mathbb{E}[y]^{\circ} \quad \text{Hence, } \mathbb{E}[y] \text{ are non-auto-correlated random signals.}$$

Suppose we, for each new value $d(y)$, encode the signal into a sum of four single-bit signals, $q_1^1$, $q_1^2$, $q_1^3$, $q_1^4$, and $q_1^5$. And $q_1^1 + q_1^2 + q_1^3 + q_1^4 = d(y)$.
This is feasible because the basis signals $\mathbf{q}$ and $\mathbf{1}$ are I-bit signals. The D/A conversions must be linear:

\[
(y)^{1b} \cdot (\sqrt{Y - 1} \mathbf{y}) + (y)^{0b} \cdot \frac{\sqrt{Y + 1}}{Y + 1} = (y)^{0b}
\]

A small DAC gain mismatch is acceptable:

\[
(y)^{2b} - (y)^{1b} = (y)^{1b}
\]

The quantization signals cancel each other:

\[
(y)^{2q} + (y)^{1q} = (y)^{0q}
\]

The input signal is decomposed into sub-siginals.
The factor by which errors are suppressed is thus: \(10^{-3} \cdot 10^{-2} = 10^{-5}\). 

In the signal band, say 1% \(\%\) will be.
When properly shaped, only a small fraction of the power will leak to the output, say 1%. 

Only a relatively small fraction of \(\gamma\) is suppressed by two factors.

The mismatch-induced error is suppressed by two factors: \(0 = (\gamma)^2 B^2\).

Mismatch-shaping encoders are generalized modulators.

The Fundamental Principle in Mismatch-Shaping.
Figures are based on $\alpha_{\text{std}} = 1\%$ (standard deviation of total DAC capacitance), 50 dB improvement at $\text{OSR} = 100$ (dithered encoder).

The noise is shaped; the SNR increases significantly with the OSR. $\text{SNR} = Nf/B$ for randomizing DACs.
Perforance Comparison

Spectrum and yield resulting from various encoding schemes $\sigma_{\text{tol}} = 1\%$
First-Order Algorithms are Preferable for OSR \geq 25

They are also characterized by a higher circuit complexity
However, they barely shape the quantization noise at higher frequencies
They are characterized by a better suppression of \( e(y) \) at low frequencies
Second-order algorithms have been developed: bounded \( (y)^2 \) bounded

First-Order Mismatches Shaping is Generally Preferable